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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)
	10/682,166	ISHIMI, KOICHI
	Examiner	**Art Unit**
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/11/05 & 05/03/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6-9,11-17,19-26,55-62 and 75-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,12,22-26,55-62 and 75-78* is/are allowed.

6)☒ Claim(s) *2-4,6,7,11,13-17,19-21 and 79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This is a reply to the Applicant's amendment submitted on 05/03/2005. By virtue of this amendment, claims 2-4, 6-9, 11-17, 19-26, 55-62 and 75-79 are now pending.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 13, the recitation "*at least one of a power supply potential and a ground potential of said buffer circuit varies using a control signal*" renders the claim indefinite since it is not clear how one of a power supply potential and a ground potential of the buffer circuit varies (using a control signal), according to Figures 1 and 7 of the claimed invention, there is no control signal shown that would provide variations in either the power supply potential or the ground potential. Clarification is required.

With respect to claim 14, the recitation "a substrate potential of a transistor included in said buffer circuit varies using a control signal" renders the claim indefinite since it is not clear how a substrate potential of a transistor included in said buffer circuit varies using a control signal (using a control signal), according to Figures 1 and 7 of the claimed invention, there is no control signal shown that would provide variations in the substrate potential. Clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yen (U.S. Patent No. 6,501,307).

With respect to claim 13, as best understood, Yen discloses, in Figs. 2, 7A and 7B, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal; and a buffering portion [20] buffering the clock signal, in which the buffering portion includes at least one buffer circuit for changing a duty ratio [shown in Fig. 7B] of the clock signal, and at least one of a power supply potential and a ground potential of the buffer circuit varies using a control signal [CTL1, CTL2].

With respect to claim 14, as best understood, Yen discloses, in Figs. 2, 7A and 7B, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal; and a buffering portion [20] buffering the clock signal, in which a substrate potential of a transistor included in buffer circuit varies using a control signal [CTL1, CTL2].

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamato et al. (U.S. Pub. No. 2001/0027503).

With respect to claim 15, Yamato et al. discloses, in Figs. 2, and 3A&B, a clock generation circuit comprising a frequency-multiplying circuit [46] receiving an input of a reference clock signal [REFCLK] and outputting a same or frequency-multiplied clock signal of said reference clock signal; and a buffering portion [200, 47, 48, 49] buffering the clock signal, the buffering portion includes at least one buffer circuit for changing a duty ratio of clock signal [Fig. 3B, item P5], clock generation circuit further comprising a delay circuit [40] capable of controlling a delay time using a delay control signal; and a logic element [44] receiving an output signal from the delay circuit and the reference clock signal for outputting a clock signal [REFSYNC].

With respect to claim 16, Yamato et al. discloses, in Figs. 2, that the logic element is an AND gate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamato et al. (U.S. Pub. No. 2001/0027503).

With respect to claim 17, Yamato et al. discloses all the claimed limitations in claim 15, and also the claimed limitation in claim 16, in which the logic element is an AND gate; Yamamato et al. fails to disclose the logic element being an OR gate. However, the conversions from an AND gate to an OR gate including an AND gate are believed to be well known; e.g. by adding inverter at each input and also at the output of the AND gate to provide equivalent functionality of an OR gate. Therefore, to configure an OR gate including an AND gate would have been deemed obvious to an artisan skilled in the art in the logic design art at the time of the invention depending on the required implementation.

8. Claims 2-4, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (U.S. Patent No. 6,501,307) in view of Proebsting (U.S. Patent No. 5,5191,344).

With respect to claim 2, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input [input] of a reference clock signal and outputting a same or frequency-multiplied clock signal [FCLK] of the reference clock signal; and a buffering portion [20] buffering the clock signal.

Yen fails to explicitly show that the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other, and the buffer circuit includes a first inverter circuit receiving the clock signal and a second inverter circuit receiving an output of the first inverter circuit, one of the first and second inverter circuits including a first transistor connected between a power supply node and an output node and having one polarity and a second transistor connected between the output node and a ground node and having the other polarity, and a gate delay amount for an input signal at the first transistor and a gate delay amount for an input signal at said second transistor are different from each other.

Proebsting discloses, in Fig. 1B, a buffer circuit for buffering a clock signal such that a logic low period and a logic high period of the clock signal are different from each other *(due to the difference in the transistor sizes)*, and the buffer circuit includes a first inverter circuit [118] receiving the clock signal and a second inverter circuit [120] receiving an output of the first inverter circuit, one of the first and second inverter circuits including a first transistor [118P] connected between a power supply node and an output node and having one polarity and a second transistor [118N] connected between the output node and a ground node and having the other polarity, and a gate delay amount for an input signal at the first transistor and a gate delay amount for an input signal at the second transistor are different from each other.

To configure the circuit of Yen with a buffer circuit as taught by Proebsting for fast propagation technique would have been obvious to one of ordinary skill in the art at the time of the invention since Proebsting teaches that such buffer circuit would reduce propagation delay times without the limitations of post charge logic *(see Proebsting, col.1, lines 49-51)*.

With respect to claim 3, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal.

Yen fails to disclose a buffering portion buffering the clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of said clock signal are different from each other, and at least one of a power supply potential or a ground potential in the buffer circuit is different from another power supply voltage or ground voltage in the buffering portion.

Proebsting discloses, in Fig. 1B, a buffer circuit for buffering a clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other *(due to the difference in the transistor sizes)*, and at least one of a power supply potential or a ground potential in the buffer circuit is different from another power supply voltage or ground voltage in the buffering portion.

To configure the circuit of Yen with a buffer circuit as taught by Proebsting for fast propagation technique would have been obvious to one of ordinary skill in the art at the time of the invention since Proebsting teaches that such buffer circuit would reduce propagation delay times without the limitations of post charge logic *(see Proebsting, col.1, lines 49-51)*.

With respect to claim 4, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of said reference clock signal.

Yen fails to disclose a buffering portion buffering the clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other, and a substrate potential of a transistor included in the buffer circuit is different from a substrate potential of another transistor included in the buffering portion.

Proebsting discloses, in Fig. 1B, a buffer circuit for buffering a clock signal, the buffering portion includes at least one buffer circuit buffering the clock signal such that a logic low period and a logic high period of the clock signal are different from each other *(due to the difference in the transistor sizes)*, and a substrate potential of a transistor included in the buffer circuit is different from a substrate potential of another transistor included in the buffering portion *(due to the difference in the transistor sizes)*.

To configure the circuit of Yen with a buffer circuit as taught by Proebsting for fast propagation technique would have been obvious to one of ordinary skill in the art at the time of the invention since Proebsting teaches that such buffer circuit would reduce propagation delay times without the limitations of post charge logic *(see Proebsting, col.1, lines 49-51)*.

With respect to claim 11, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input [input] of a reference clock signal and outputting a same or frequency-multiplied clock signal [FCLK] of the reference clock signal; and a buffering portion [20] buffering the clock signal.

Yen fails to explicitly show that the buffering portion includes at least one buffer circuit for changing a duty ratio of the clock signal, the buffer circuit includes a first inverter circuit receiving the clock signal, and a second inverter circuit receiving an output of the first inverter circuit, one of the first and second inverter circuits including a plurality of first transistors connected in parallel between a power supply node and an output node and having one polarity, a plurality of second transistors connected in parallel between the output node and a ground node and having the other polarity, and a driving capability control portion controlling on/off of the plurality of first and second transistors respectively using a plurality of driving capability control signals.

Proebsting discloses, in Fig. 1B, a buffer circuit for buffering a clock signal, for changing a duty ratio of the clock signal, the buffer circuit includes a first inverter circuit [118] receiving the clock signal, and a second inverter circuit [120] receiving an output of the first inverter circuit, one of the first and second inverter circuits including a plurality of first transistors connected in parallel between a power supply node and an output node and having one polarity, a plurality of second transistors connected in parallel between the output node and a ground node and having the other polarity, and a driving capability control portion controlling on/off of the plurality of first and second transistors respectively using a plurality of driving capability control signals.

To configure the circuit of Yen with a buffer circuit as taught by Proebsting for fast propagation technique would have been obvious to one of ordinary skill in the art at the time of the invention since Proebsting teaches that such buffer circuit would reduce propagation delay times without the limitations of post charge logic *(see Proebsting, col.1, lines 49-51)*.

9. Claims 6 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (U.S. Patent No. 6,501,307) in view of Lane (U.S. Patent No. 5,771,264).

With respect to claims 6 and 19, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal, the clock signal having a logic high period and a logic low period different from each other [Fig. 7B]; and a buffering portion [20] buffering the clock signal.

Yen fails to teach the frequency-multiplied circuit includes a) a ring oscillator, b) a comparator comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter determining a digital count value based on a phase comparison result output from the comparator, and d) a control circuit incrementing/decrementing the digital count value in response to a rising/falling of the clock signal, the ring oscillator including a delay line varying a delay time in accordance with the digital count value.

Lane discloses, in Fig. 1, a frequency multiplier including a) a ring oscillator [12], b) a comparator [22] comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter [24] determining a digital count value based on a phase comparison result output from the comparator, and d) a control circuit [16] incrementing/decrementing the digital count value in response to a rising/falling of the clock signal when a count value control signal has a prescribed value, the ring oscillator including a delay line varying a delay time in accordance with the digital count value.

To configure the circuit of Yen with a frequency multiplier as taught by Lane with simple architecture would have been obvious to one of ordinary skill in the art at the time of the invention since Lane teaches that such configuration of the frequency multiplier provides synchronously reproducing a clock signal which is a selective frequency multiple of the input clock signal *(see Lane, col. 1, lines 49-51).*

With respect to claim 20, the combination of Yen and Lane discloses that the count value control signal takes the prescribed value is determined in accordance with the digital count value.

With respect to claim 21, the combination of Yen and Lane discloses that whether the count value control signal takes the prescribed value is determined in accordance with a frequency of the clock signal.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (U.S. Patent No. 6,501,307) in view of Suda (U.S. Pub. No. 2004/0247066).

With respect to claim 7, Yen discloses, in Fig. 2, a clock generation circuit comprising a frequency-multiplying circuit [14] receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of the reference clock signal, the clock signal having a logic high period and a logic low period different from each other [Fig. 7B]; and a buffering portion [20] buffering the clock signal.

Yen fails to teach the frequency-multiplied circuit includes a) a ring oscillator, b) a comparator comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter determining a digital count value based on a phase comparison result output from the comparator, and the ring oscillator including first and second delay lines connected in series for receiving the digital count value for determining a delay time, and a selector selecting and outputting an input from one of the first and second delay lines in accordance with said clock signal.

Suda discloses, in Figs. 1 and 16, paragraph [0264], lines 6-8, a frequency multiplier including a) a ring oscillator [3], b) a comparator [1] comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter [2] determining a digital count value based on a phase comparison result output from the comparator, and the ring oscillator including first and second delay lines *(from 115)* connected in series for receiving the digital count value for determining a delay time, and a selector [116] selecting and outputting an input from one of the first and second delay lines in accordance with said clock signal.

To configure the circuit of Yen with a frequency multiplier as taught by Suda which have small power consumption would have been obvious to one of ordinary skill in the art at the time of the invention since Suda teaches that such configuration of the frequency multiplier can be readily reduced in size, enable a locked loop in a high band and have high reliability *(see Suda, paragraph [0023], lines 3-5).*

11. Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting (U.S. Patent No. 5,519,344) in view of Lane (U.S. Patent No. 5,771,264).

With respect to claim 79, Proebsting discloses, in Fig. 1B, a buffering portion [118, 120, 122, 124] including at least one buffer circuit for changing duty ratio of a clock signal.

Proebsting fails to discloses a frequency-multiplying circuit to provide the clock signal, the frequency-multiplying circuit receiving an input of a reference clock signal and outputting a same or frequency-multiplied clock signal of a reference clock signal; the frequency-multiplying circuit includes a ring oscillator, a comparator comparing a phase of said clock signal output from said ring oscillator with a phase of said reference clock signal, a counter determining a digital count value based on a phase comparison result output from the comparator, and a control circuit incrementing/decrementing the digital count value in accordance with a rising/falling of the clock signal when a count value control signal has a prescribed value, the ring oscillator including a delay line varying a delay time in accordance with the digital count value.

Lane discloses, in Fig. 1, a frequency multiplier for generating a clock signal including a) a ring oscillator [12], b) a comparator [22] comparing a phase of the clock signal output from the ring oscillator with a phase of the reference clock signal, c) a counter [24] determining a digital count value based on a phase comparison result output from the comparator, and d) a control circuit [16] incrementing/decrementing the digital count value in response to a rising/falling of the clock signal when a count value control signal has a prescribed value, the ring oscillator including a delay line varying a delay time in accordance with the digital count value.

To configure the circuit of Proebsting with a clock signal provides by a frequency multiplier as taught by Lane with simple architecture would have been obvious to one of ordinary skill in the art at the time of the invention since Lane teaches that such configuration of the frequency multiplier provides synchronously reproducing a clock signal which is a selective frequency multiple of the input clock signal *(see Lane, col. 1, lines 49-51).*

Allowable Subject Matter

12. Claims 8-9, 12, 22-26, 55-62, 75-78 are allowed.

13. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 8;

b) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low is different from the other period of time, in combination with the remaining claimed limitations, as called for in claim 9;

c) A clock generation circuit, in which a timing control portion controlling rising or falling timing of a signal level output from a first inverter circuit to a second inverter circuit using a plurality of timing control signals, in combination with the remaining claimed limitations, as called for in claim 12;

d) A clock generation circuit, in which a logic element receiving a selector control signal and a clock signal for outputting a select signal, in combination with the remaining claimed limitations, as called for in claim 22;

e) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic high and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 25;

f) A clock generation circuit, in which in a duty ratio control signal, a period of time during which both of clock signal and the duty ratio control signal are logic low and the other period of time varies, in combination with the remaining claimed limitations, as called for in claim 26;

g) A system including a current measurement circuit measuring an operating current of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the operating current, in combination with the remaining claimed limitations, as called for in claims 55 and 56;

h) A system including a temperature measurement circuit measuring a temperature of a circuit receiving clock signal, in which a central processing unit controls a duty ratio of the clock signal or on/off of duty ratio control based on a measurement result of the temperature, in combination with the remaining claimed limitations, as called for in claims 59 and 60; and

i) A system, in which a duty ratio of a clock signal can be set by an instruction from a central processing unit, individually for the clock signal being supplied to a module circuit and for the clock signal being supplied to a prescribed external circuit, in combination with the remaining claimed limitations, as called for in claims 75 and 76.

Remarks

14. Applicant is noted that claims 3-4, 6-7, 11, 15-17, 19-21 and 79 have been rejected in view of the new ground(s) of rejection or newly found prior art; thus previously indicated allowable subject matters have been withdrawn.

Regarding Applicant's arguments filed 04/11/2005 with respect to claims 3-4 on page 26, fourth paragraph, the Applicant stated that reference to Yen, "*this reference does not disclose to change a potential of a buffer circuit itself*", it is noted that the features upon which applicant relies are not recited in the rejected claims 3 and 4. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding Applicant's arguments filed 04/11/2005 with respect to claims 13-14 on page 26, fourth paragraph, the Applicant stated that reference to Yen, "*this reference does not disclose to change a potential of a buffer circuit itself*", see 112 2nd paragraph set forth in the office action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER